



AMENDMENT UNDER 37 C.F.R. § 1.312

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Title: CONTROLLER FOR DELAY LOCKED LOOP CIRCUITS

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IN THE CLAIMS

1. (Previously Presented) A memory device comprising:
a delay locked loop (DLL) for generating an internal clock signal based on an external clock signal, the DLL keeping the external and internal clock signals synchronized by performing a synchronization operation; and
a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from performing the synchronization operation during the test mode.
2. (Original) The memory device of claim 1 further comprising a plurality of memory cells for storing data.
3. (Original) The memory device of claim 2, wherein during the test mode, the memory cells are activated in preparation for subsequent access to the memory cells.
4. (Original) The memory device of claim 2, wherein during the test mode, the memory cells are accessed for reading the data stored in the memory cells.
5. (Original) The memory device of claim 2, wherein during the test mode, the memory cells are refreshed to ensure the memory cells retain valid data values.
6. (Previously Presented) The memory device of claim 1, wherein the DLL includes:
a phase detector for comparing the external and internal clock signals to activate a shifting signal when the external and internal clock signals are not synchronized; and
a shift register for performing a shifting operation based on the shifting signal to keep the external and internal clock signals synchronized.

7. (Currently Amended) The memory device of claim 6, wherein the DLL controller includes:

- a test mode select input for receiving a select signal during the test mode;
- a test mode control input for receiving a test control signal during the test mode; and
- an output connected to the DLL for providing the DLL control signal, wherein during the test mode, the activation of the DLL control signal is based on the test control signal and ~~in~~ responding to the select signal.

8. (Previously Presented) A memory device comprising:

- a delay locked loop (DLL) for applying a delay to an external clock signal to generate an internal clock signal, the DLL adjusting the delay to keep the external and internal clock signals synchronized; and

- a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from adjusting the delay during the test mode.

9. (Original) The memory device of claim 8 further comprising a plurality of memory cells, wherein during the test mode, the memory cells are activated in preparation for subsequent access to the memory cells.

10. (Original) The memory device of claim 8 further comprising a plurality of memory cells, wherein during the test mode, the memory cells are accessed for reading data stored in the memory cells.

11. (Original) The memory device of claim 8 further comprising a plurality of memory cells, wherein during the test mode, data in stored in the memory cells are refreshed to ensure the memory cells retain valid data values.

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12. (Original) The memory device of claim 8, wherein the DLL includes:
- a phase detector for comparing the external and internal clock signals to activate a shifting signal when the external and internal clock signals are not synchronized; and
 - a shift register for adjusting the delay based on the shifting signal to keep the external and internal clock signals synchronized.
13. (Currently Amended) The memory device of claim 8, wherein the DLL controller includes:
- a test mode select input for receiving a select signal during the test;
 - a test mode control input for receiving a test control signal during the test; and
 - an output connected to the DLL for providing the DLL control signal, wherein during the test mode, the activation of the DLL control signal is based on the test control signal and ~~in~~ responding to the select signal.
14. (Previously Presented) A memory device comprising:
- a plurality of inputs for receiving a plurality of input signals and an external clock signal;
 - a delay locked loop (DLL) for generating an internal clock signal based on the external clock signal, the DLL performing a shifting operation to keep the external and internal clock signals synchronized;
 - a decode circuit for activating a test mode signal based on a certain combination of the input signals to initiate a test mode of the memory device; and
 - a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal to disable the shifting operation during the test mode.
15. (Original) The memory device of claim 14 further comprising a plurality of memory cells, wherein during the test mode, the memory cells are being activated for subsequent access to the memory cells.

16. (Previously Presented) The memory device of claim 14, wherein the DLL includes a delay line having a plurality of delay stages connected in series for applying an amount of delay to the external clock signal to generate the internal clock signal.

17. (Previously Presented) The memory device of claim 14, wherein the DLL further includes:

a phase detector for comparing the external and internal clock signals to activate a shifting signal when the external and internal clock signals are not synchronized; and

a shift register for adjusting the amount of delay based on the shifting signal to keep the external and internal clock signals synchronized.

18. (Currently Amended) The memory device of claim 14, wherein the DLL controller includes:

a test mode select input for receiving a select signal during the test;

a test mode control input for receiving a test control signal during the test; and

an output connected to the DLL for providing the DLL control signal, wherein during the test mode, the activation of the DLL control signal is based on the test control signal and ~~in~~ responding to the select signal.

19. (Currently Amended) A memory device comprising:

a delay line for applying an amount of delay to the external clock signal to generate the internal clock signal;

a phase detector for comparing the external and internal clock signals to activate a shifting signal when the external and internal clock signals are not synchronized;

a shift register for performing a shifting operation to adjust the amount of delay based on the shifting signal to keep the external and internal clock signals synchronized;

a test mode select input for receiving a test select signal;

a test mode control input for receiving a test control signal; and

an output connected to the phase detector providing the DLL control signal for selectively ~~disable~~ disabling the shifting operation based on the test select signal and the test control signal during a test mode.

20. (Currently Amended) The memory device of claim 19, wherein the phase detector includes:

input latches for receiving the external clock signal and a feedback signal to provide a first phase signal and a second phase signal, the feedback signal being a delayed version of the internal clock signal;

a logic circuit connected to the input latches for receiving the first and second phase signals to generate pre-shifting signals;

output latches for activating shifting signals based on the pre-shifting signals when the external and internal clock signals are not synchronized; and

[[and]] a shifting signal control circuit for deactivating the shifting signals during the test mode.

21. (Previously Presented) A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a delay locked loop (DLL) for generating an internal clock signal based on an external clock signal, the DLL keeping the external and internal clock signals synchronized by performing a synchronization operation; and

a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from performing the synchronization operation during the test mode.

22. (Original) The system of claim 21 further comprising a plurality of memory cells for storing data.

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23. (Original) The system of claim 21, wherein during the test mode, the memory cells are activated in preparation for subsequent access to the memory cells.
24. (Original) The system of claim 21, wherein during the test mode, the memory cells are accessed for reading the data stored in the memory cells.
25. (Original) The system of claim 21, wherein during the test mode, the data in the memory cells are refreshed to ensure the memory cells retain valid data values.
26. (Previously Presented) A system comprising:
a processor; and
a memory device connected to the processor, the memory device including:
a delay locked loop (DLL) for applying a delay to an external clock signal to generate an internal clock signal, the DLL adjusting the delay to keep the external and internal clock signals synchronized; and
a DLL controller having a selector connected to the DLL for selectively activating a DLL control signal during a test mode of the memory device to prevent the DLL from adjusting the delay during the test mode.
27. (Original) The system of claim 26 further comprising a plurality of memory cells arranged in rows and columns.
28. (Original) The system of claim 26, wherein in the test mode, a row of the memory cells is activated in preparation for subsequent access to the memory cells.
29. (Original) The system of claim 26, wherein in the test mode, a column of the memory cells is activated in preparation for subsequent access to the memory cells.
- 30-41. (Canceled)

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42. (Previously Presented) A memory device comprising:
- an input for receiving an external clock signal;
 - a delay locked loop (DLL) for generating an internal clock signal based on the external clock signal, the DLL having a synchronization operation for keeping the external and internal clock signals synchronized; and
 - a DLL controller having a selector connected to the DLL for generating a DLL control signal independently from the external clock signal during a test mode of the memory device to disable the synchronization operation for a suspension time during the test mode.
43. (Previously Presented) The memory device of claim 1, wherein the DLL includes:
- a phase detector for comparing the external and the internal clock signals to activate a shifting signal when the external and internal clock signals are not synchronized; and
 - a shift register for performing the shifting operation based on the shifting signal to keep the external and internal clock signals synchronized.
44. (Previously Presented) The memory device of claim 42, wherein the selector includes a multiplexor for selecting between an active mode signal generated before the test mode and a test control signal generated during the test mode as the DLL control signal based on a test select signal.
45. (Currently Amended) A memory device comprising:
- an input for receiving an external clock signal;
 - a delay locked loop (DLL) having a delay line for applying a delay to the external clock signal to generate an internal clock signal, and having a shift register for adjusting the delay based on a shifting signal; and
 - a DLL controller having a selector connected to the DLL for activating a DLL control signal independently from the external clock signal during a test mode of the memory device to prevent the shift register from adjusting the delay during the test mode.

46. (Previously Presented) The memory device of claim 45, wherein the DLL further includes:

a phase detector for comparing the external and the internal clock signals to activate the shifting signal when the external and internal clock signals are not synchronized.

47. (Previously Presented) The memory device of claim 45, wherein the selector includes a multiplexor for selecting between an active mode signal generated before the test mode and a test control signal generated during the test mode as the DLL control signal based on a test select signal.

48. (Previously Presented) A memory device comprising:

a plurality of inputs for receiving a plurality of input signals and an external clock signal;
a delay locked loop (DLL) for generating an internal clock signal based on the external clock signal, the DLL having a shifting operation to keep the external and internal clock signals synchronized;

a decode circuit for activating a test mode signal based on a certain combination of the input signals to initiate a test mode of the memory device; and

a DLL controller having a selector connected to the DLL for activating a DLL control signal independently from the external clock signal to disable the shifting operation during the test mode.

49. (Previously Presented) The memory device of claim 48, wherein the DLL includes:

a phase detector for comparing the external and the internal clock signals to activate a shifting signal when the external and internal clock signals are not synchronized; and

a shift register for performing the shifting operation based on the shifting signal to keep the external and internal clock signals synchronized.

50. (Previously Presented) The memory device of claim 48, wherein the selector includes a multiplexor for selecting between an active mode signal generated before the test mode and a test

control signal generated during the test mode as the DLL control signal based on a test select signal.

51. (Previously Presented) A system comprising:

a processor; and

a memory device connected to the processor, the memory device including:

a plurality of inputs for receiving a plurality of input signals and an external clock signal;

a delay locked loop (DLL) for generating an internal clock signal based on the external clock signal, the DLL having a shifting operation to keep the external and internal clock signals synchronized;

a decode circuit for activating a test mode signal based on a certain combination of the input signals to initiate a test mode of the memory device; and

a DLL controller having a selector connected to the DLL for activating a DLL control signal independently from the external clock signal to disable the shifting operation during the test mode.

52. (Previously Presented) The system of claim 51, wherein the DLL includes:

a phase detector for comparing the external and the internal clock signals to activate a shifting signal when the external and internal clock signals are not synchronized; and

a shift register for performing the shifting operation based on the shifting signal to keep the external and internal clock signals synchronized.

53. (Previously Presented) The system of claim 51, wherein the selector includes a multiplexor for selecting between an active mode signal generated before the test mode and a test control signal generated during the test mode as the DLL control signal based on a test select signal.